drive control element DR. The gate of the diode-connecting switch SWc is connected to the scan signal line SL**2**.

[**0038**] The capacitor C is connected between a constant-potential terminal and the gate of the drive control element DR. In this embodiment, the capacitor C is connected between the first power supply terminal ND**1** and the gate of the drive control element DR.

[**0039**] A protection circuit PC**1** is connected to each video signal line DL. The protection circuit PC**1** includes diodes D**1***a* and D**1***b*. The diode D**1***a* is connected between the video signal line DL and a high-potential terminal NDH such that a forward current flows through the diode D**1***a* from the video signal line DL to the high-potential terminal NDH. A potential of the high-potential terminal NDH is to be set higher than that of the video signal line DL. The diode D**1***b* is connected between the video signal line DL and a low-potential terminal NDL such that a forward current flows through the diode D**1***a* from the high-potential terminal NDH to the video signal line DL. A potential of the low-potential terminal NDL is to be set lower than that of the video signal line DL. In this embodiment, the diode D**1***a* is a p-channel thin-film transistor whose gate is connected to the high-potential terminal NDH, and the diode D**1***b* is an n-channel thin-film transistor whose gate is connected to the low-potential terminal NDL.

[**0040**] The video signal line driver XDR is mounted on the display panel DP. As shown in **FIG. 3**, the video signal line driver XDR includes a current source CS, a switch SWvs, and a protection circuit PC**2** for each video signal line DL. The video signal line driver XDR further includes multiplexer MLT, a voltage source VS, a reference transistor $TR_{ref}$, and a control line CL.

[**0041**] The multiplexer MLT includes input terminals to which a clock signal CLK, a start signal START, a video signal DATA as a serial signal are supplied. The multiplexer MLT further includes output terminals for each current source CS. The multiplexer MLT converts the video signal DATA from a serial signal into parallel signals under control of the clock signal CLK and the start signal START, and outputs the parallel signals to each current source CS. In this embodiment, the multiplexer MLT outputs the video signal as a 6-bit digital signal to each current source CS.

[**0042**] The reference transistor $TR_{ref}$ is a p-channel thin-film transistor in this embodiment. A source of the reference transistor $TR_{ref}$ is connected to a constant-potential terminal ND**1**' via a resistance element R. A drain of the reference transistor $TR_{ref}$ is connected to a ground wire. When driving the display, a reference current $I_{ref}$ is made to flow between the source and drain of the reference transistor $TR_{ref}$.

[**0043**] The current source CS is connected between an output terminal of the video signal line driver XDR, i.e., the terminal connected to the video signal line, and the ground wire. The current source CS converts the digital signal which the multiplexer MLT output as parallel signals into an analog signal. In this embodiment, the current source CS converts the 6-bit digital video signal which the multiplexer MLT outputs into the analog video signal as a current signal.

[**0044**] The current source CS includes a plural sets of a constant-current source $TR_{dgt}$ and a switch $SW_{dgt}$. The constant-current source $TR_{dgt}$ and the switch $SW_{dgt}$ of each set are connected in series between the output terminal of the video signal line driver XDR and the ground wire. In this embodiment, the current source CS includes six sets of the constant-current source $TR_{dgt}$ and the switch $SW_{dgt}$, and the constant-current sources $TR_{dgt}$ and the switches $SW_{dgt}$ are p-channel field-effect transistors.

[**0045**] Gates of the constant-current sources $TR_{dgt}$ are connected to a gate of the reference transistor $TR_{ref}$. Gate of the switches $SW_{dgt}$ are connected to the output terminals of the multiplexer MLT, respectively.

[**0046**] For example, one of the constant-current sources $TR_{dgt}$ has the same structure as that of the reference transistor $TR_{ref}$, and the remaining five have the same structure as that of the reference transistor $TR_{ref}$ except for channel width. The six constant-current sources $TR_{dgt}$ output constant-currents having magnitudes one time, two times, four times, eight times, sixteen times, and thirty two times the magnitude of the reference current $I_{ref}$, respectively, while the switches $SW_{dgt}$ are closed.

[**0047**] The switch $SW_{vs}$ and the voltage source VS are connected in series between the output terminal of the video signal line driver XDR and the ground wire in this order.

[**0048**] The voltage source VS outputs a reset signal as a constant-voltage. For example, an output of the voltage signal VS is a constant-voltage almost equal to the voltage of the video signal line DL to be set by a write operation when the video signal corresponds to the lowest gray level.

[**0049**] In this embodiment, the switch $SW_{vs}$ is a p-channel field-effect transistor. A gate of the switch $SW_{vs}$ is connected to the control line CL. The control line CL is supplied with a control signal BLK whose signal level changes almost in synchronization with changeovers between a blanking period and an effective scanning period.

[**0050**] The protection circuit PC**2** is connected to the output terminal of the video signal line driver XDR. The protection circuit PC**2** includes diodes D**2***a* and D**2***b*. The diode D**2***a* is connected between the output terminal of the video signal line driver XDR and a high-potential terminal NDH' such that a forward current flows through the diode D**2***a* from the output terminal of the video signal line driver XDR to the high-potential terminal NDH'. A potential of the high-potential terminal NDH' is to be set higher than that of the output terminal of the video signal line driver XDR. The diode D**2***b* is connected between the output terminal of the video signal line driver XDR and a low-potential terminal NDL' such that a forward current flows through the diode D**2***a* from the low-potential terminal NDL' to the output terminal of the video signal line driver XDR. A potential of the low-potential terminal NDL' is to be set lower than that of the output terminal of the video signal line driver XDR. In this embodiment, The diode D**2***a* is a p-channel field-effect transistor whose gate is connected to the high-potential terminal NDH', and the diode D**2***b* is an n-channel field-effect transistor whose gate is connected to the ground wire.

[**0051**] The scan signal line driver YDR is further mounted on the display panel DP. As described above, the scan signal lines SL**1** and SL**2** are connected to the scan signal line driver YDR.

[**0052**] The organic EL display is driven by, for the example, the method described below.